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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
BATTAGLIA, MICHAEL V

ART UNIT	PAPER NUMBER
2652	4

DATE MAILED: 09/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,837	SHIGEMORI, TOSHIHIRO	
	Examiner	Art Unit	
	Michael V Battaglia	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4* is/are rejected.

7)☒ Claim(s) *2,3,5,and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to because Fig. 6 has the following informalities:

a. The examiner requests replacing the label "d CNT" of the 4-bit counter 451 with -A CNT-.

b. The examiner suggests replacing "D1", the data input label of counters 451 and 452, with -Di- to match the specification.

c. The examiner suggests replacing "Q", the value inputted to the data input of counter B, with -0- to match the specification.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The disclosure is objected to because of the following informalities:

a. On page 21, line 4, the examiner suggests replacing "input L" with -input LD- so that the specification is consistent with Fig. 6 of the drawings.

b. On page 23, lines 7-10 need to be rewritten because the divided clock counter 46 shown in Fig. 6 does not input both the 2-bit count data and the 2-bit frequency dividing condition setting value into the frequency dividing rate setting table 47. The examiner suggests rewriting the sentence as -2-bit count data from the divided clock counter 46 and 2-bit data as the frequency dividing condition setting value are inputted into the frequency dividing rate setting table 47.-

c. On page 23, lines 13-14 need to be rewritten for the same reason stated above. The examiner suggests -based on the count value of the divided clock counter 46 and the frequency dividing condition setting value.-

d. On page 30, line 11, the examiner suggests replacing "contact" with -constant-.

Appropriate correction is required.

Claim Objections

5. Claim 5 and therefor 6 are objected to because of the following informality: Claim 5 claims "a wobble signal cycle counting unit that counts cycles of the divided wobble signal by the cycle of the recording clock signal." However, the specification, on page 43, line 17 through page 18, line 4 and in Fig. 15, describes a divided recording clock counting unit that count cycles of the divided recording clock by the cycle of the divided wobble signal. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Saito et al (US 5,377,178) (hereafter Saito).

Saito discloses a data recording clock signal generator (Col. 28, lines 23-61) that generates a recording clock signal synchronous with a wobble signal used for recording data on an optical disk having a data recording track wobbled by the wobble signal having predetermined frequency components (Col. 3, lines 40-46 and Col. 5, lines 35-43), said data recording clock generator comprising: a wobble signal extracting unit that extracts the wobble signal (Fig. 3 and Fig. 15, element 606); a recording clock signal dividing unit that generates a divided clock signal obtained by dividing the frequency of the recording clock signal (Fig. 24, element 1210); a phase difference signal generating unit that generates a phase difference signal as a result of phase comparison between the wobble signal and the divided clock signal (Fig. 24, element 1200); a frequency control signal generating unit that generates a frequency control signal based on the phase difference signal generated by the phase difference signal generating unit (Fig. 24, elements 1202 and 1204); and a recording clock signal generating unit that generates the recording clock signal having a frequency

controlled in accordance with the frequency control signal generated by the frequency control signal generator (Fig. 15, element 610 and Fig. 24, element inside the dashed lines), wherein the recording clock signal dividing unit is provided with a frequency dividing rate setting unit that sets a reference frequency dividing rate by which the frequency of the recording clock signal is divided and a frequency dividing rate different from the reference frequency dividing rate, following predetermined procedures (Fig. 24, elements 1212 and 1214). The examiner interprets the initial frequency dividing rate as the reference frequency dividing rate and the frequency dividing rates different from the initial frequency dividing rate as being frequency dividing rates different from the reference frequency dividing rate. The examiner notes that the PLL circuit of Fig. 24 inherently has an initial frequency dividing rate because an initial frequency dividing rate is needed for the PLL to be a stable oscillating source.

7. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Fushima et al (US 6,088,307) (hereafter Fushima).

Fushima discloses a data recording clock signal generator that generates a recording clock signal synchronous with a wobble signal used for recording data on an optical disk having a data recording track wobbled by the wobble signal, which has predetermined frequency components (Col. 4, lines 15-19 and Fig. 1), and on which address information and a synchronizing signal are phase-modulated and superimposed (Col. 1, lines 26-30 and Col. 4, 15-19), said data recording clock signal generator comprises: a wobble signal extracting unit that extracts the wobble signal (Figs. 5-6, element 41); a recording clock signal dividing unit that generates a divided clock signal obtained by dividing a frequency of the recording clock signal (Fig. 6, element 56); a phase difference signal generating unit that

generates a phase difference signal as a result of a phase comparison between the wobble signal and the divided clock signal (Fig. 6, element 95); a frequency control signal generating unit that generates a frequency control signal based on the phase difference signal generated by the phase difference signal generating unit (Fig. 6, elements 96-97); a recording clock signal generating unit that generates the recording clock signal having a frequency controlled in accordance with the frequency control signal generated by the frequency control signal generating unit (Fig. 6, element 55); and a masking unit that prevents the phase difference signal generating unit from generating the phase difference signal at any timing close to the timing when either the address information or the synchronizing signal is phase-modulated on the optical disk (Figs. 5-6, element 35 and Col. 11, lines 7-18).

Citation of Relevant Prior Art

Kuroda et al (US 6,081,490) discloses adjusting a clock signal for recording information based on a phase adjusting signal produced by comparing the phases of a wobble signal and a prepit signal. Okanishi (US 6,195,325) discloses a recording clock signal dividing unit that generates a divided clock signal obtained by dividing the frequency of the recording clock signal (Fig. 20, element 56b) and a frequency dividing rate setting unit that provides a reference frequency dividing unit and a different frequency dividing rate (Fig. 20, element 70a and Col. 15, lines 24-33). Kuroda (US 6,522,608) discloses a synchronous detection unit that detects a synchronizing signal superimposed on the wobble signal (Fig. 6, element 69) and a variable recording clock signal dividing unit that generates a divided clock signal obtained by dividing the frequency of the recording clock signal (Fig.

6, element 74). Van Den Enden et al (US 6,469,968) discloses varying the process of rewriting to extend the life of an information carrier by shifting the initial write position or by scrambling the written information (Abstract). Kobayashi (US 6,252,836) discloses a variable frequency divider that divides a recording clock at a rate set by a system controller (Fig. 6, element 29d) and a cluster counter that counts wobble cycles (Fig. 6, element 30). Hikima (US 6,091,682) discloses a zero detection unit that detects a wobbling signal with no prepit signal for five successive cycles (Fig. 8, element 40 and Col. 10, lines 65-68), two wobble counters (Fig. 8, elements 41-42), and a circuit that compares the result of the counters (Fig. 8, element 43).

Allowable Subject Matter

8. Claims 2-3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In regard to claim 2, none of the references alone or in combination disclose or suggest a frequency dividing rate setting unit that changes the order of combination of the frequency dividing rates every time data recording is performed.

In regard to claim 3, none of the references alone or in combination disclose or suggest a control unit that changes a frequency dividing rate of the recording clock in relation to a reference frequency dividing rate according to whether or not a synchronous judgment circuit (phase comparator) judges that recording data is lagging behind or ahead of a wobbling synchronizing signal.

9. Claims 5-6 are allowable over prior art. The examiner notes that claim 5 currently claims "a wobble signal cycle counting unit that counts cycles of the divided wobble signal by the cycle of the recording clock signal" that is not disclosed in the detailed description or figures. None of the references alone or in combination disclose or suggest a recording clock signal generating unit that generates a recording clock signal having a frequency controlled by a signal based on a count of cycles of a divided wobble signal outside of a predetermined range and controlled by a signal based on a phase difference between a wobble signal and a divided clock signal inside of a predetermined range.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Michael Battaglia

HOA T. NGUYEN
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9/22/03